U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/29	
Application Number: 09/494,567	Filing Date: January 13, 2000	Examiner: Tonia L. Meonske	Art Unit: 2183
Invention Title: RUN-TIME RECONFIGURATION METHOD FOR PROGRAMMABLE UNITS		Inventor: VORBACH et al.	

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on

Date: 21 Sept 2006 Reg. No. 36,098

Signature: _____
Michelle M. Carniaux

SIR:

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 35 U.S.C. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant hereby brings the following references to the attention of the Examiner. These references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

2. The filing of this Information Disclosure Statement and the enclosed PTO 1449 shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. §1.56(b).

3. A copy of each patent, publication or other information listed on the modified PTO 1449 is enclosed, except where indicated on the list of references (Form 1449).

4. It is believed that no fees are due in connection with this Information Disclosure Statement. However, should any fees be due, the Commissioner is authorized to charge Deposit Account No. 11-0600 for such fees. A duplicate of this communication is enclosed for charging purposes.

Respectfully submitted,

Dated: September 21, 2006

By: Michelle M. Carniaux (Reg. No. 36,098)

CUSTOMER NUMBER 26646

KENYON & KENYON LLP
One Broadway
New York, N.Y. 10004
(212) 425-7200 (telephone)
(212) 425-5288 (facsimile)

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/29	Serial No. 09/494,567
	Applicant(s) VORBACH et al.	
	Filing Date January 31, 2000	Group Art Unit 2181

U. S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT PUBLICATION NUMBER	PATENT PUBLICATION DATE	NAME	CLASS	SUB CLASS	FILING DATE*
A	6,697,979	February 24, 2004	Vorbach et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO
B	0 726 532	August 14, 1996	EPO				

	OTHER DOCUMENTS
EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
1	Myers, G. "Advances in Computer Architecture," Wiley-Interscience Publication, 2nd ed., John Wiley & Sons, Inc. , 1978, pp. 463-494.
2	M. Saleeba, "A Self-Contained Dynamically Reconfigurable Processor Architecture," Sixteenth Australian Computer Science Conference, ASCS-16, QLD, Australia, February, 1993, pp. 59-70.
3	Maxfield, C. "Logic that Mutates While-U-Wait" EDN (Bur. Ed) (USA), EDN (European Edition), 7 November 1996, Cahners Publishing, USA, pp. 137-140, 142.
4	Baumgarte, V., et al., PACT XPP "A Self-reconfigurable Data Processing Architecture," PACT Info. GMBH, Munchen Germany, 2001, 7 pages.
5	Jantsch, Axel et al., "A Case Study on Hardware/software Partitioning," Royal Institute of Technology, Kista, Sweden, April 10, 1994 IEEE, pp. 111-118.
6	Becker, J. et al., "Parallelization in Co-compilation for Configurable Accelerators - a Host/accelerator Partitioning Compilation Method," proceedings of Asia and South Pacific Design Automation Conference, Yokohama, Japan, February 10-13, 1998, 11 pages.
7	Isshiki, Tsuyoshi et al., "Bit-Serial Pipeline Synthesis for Multi-FPGA Systems with C++ Design Capture," 1996 IEEE, pp. 38-47.
8	Weinhardt, Markus, "Ubersetzingsmethoden fur strukturprogrammierbare rechner ," Dissertation for Doktors der Ingenieurwissenschaften der Universitat Karlsruhe: July 1, 1997 [Weinhardt, M. "Compilation Methods for Structure-programmable Computers", dissertation, ISBN 3-89722-011-3, 1997], 154 pages.*
9	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
10	Weinhardt, Markus et al., "Pipeline Vectorization for Reconfigurable Systems", 1999, IEEE, pages 52-62.
11	Hammes, Jeff et al., "Cameron: High Level Language Compilation for Reconfigurable Systems," Department of Computer Science, Colorado State University, Conference on Parallel Architectures and Compilation Techniques, October 12-16, 1999, 9 pages.
12	Wada et al., "A Performance Evaluation of Tree-based Coherent Distributed Shared Memory" Proceedings of the Pacific RIM Conference on Communications, Comput and Signal Processing, Victoria, May 19-21 1993, pp. 390-393.

*** Citation #9, the Weinhardt et al. IEEE February 2001 article, is a representative technical disclosure for this Weinhardt dissertation.**

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. **2885/29**	Serial No. **09/494,567**
	Applicant(s) **VORBACH et al.**	
	Filing Date **January 31, 2000**	Group Art Unit **2181**

	OTHER DOCUMENTS
EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
13	Mirsky, E. DeHon, "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, 1996, pp. 157-166.
14	Cardoso, J.M.P., "Compilation of Java™ Algorithms onto Reconfigurable Computing Systems with Exploitation of Operation-Level Parallelism," Ph.D. Thesis, Universidade Tecnica de Lisboa (UTL), Lisbon, Portugal October 2000 **(Table of Contents and English Abstract only).**
15	XLINX, "Logic Cell Array Families: XC4000, XC4000A and XC4000H," product description, pp. 2-7, 2-9, 2-14, 2-15, 8-16, and 9-14.
16	Hauser, J.R. et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor", University of California, Berkeley, IEEE, 1997, pages 24-33.
17	Iseli, C., et al. "A C++ Compiler for FPGA Custom Execution Units Synthesis," IEEE. 1995, pp. 173-179.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.